

# Claims

- [c1] 1. A semiconductor field-effect device structure comprising:  
a host structure further comprising a channel region;  
and  
an engineered array of at least one impurity disposed at the channel region of the host structure such that component atoms of the engineered array are substantially fixed by substantially controlled placement in order to provide substantial control of carrier flow.
- [c2] 2. The semiconductor field-effect device structure of claim 1 further comprising:  
a source region;  
a drain region;  
a first insulator disposed atop the source region, the drain region, the channel region, and the engineered array; and  
a gate disposed atop the first insulator so that a field-effect transistor is formed from the semiconductor field-effect device structure.
- [c3] 3. The semiconductor field-effect device structure of claim 2 wherein the semiconductor field-effect device

structure is comprised primarily of silicon, and further comprising a second insulator disposed beneath the semiconductor field-effect device structure to form a silicon-on-insulator field-effect device.

- [c4] 4. The semiconductor field-effect device structure of claim 1 wherein the engineered array further comprises at least some of the component atoms arranged substantially in at least one row.
- [c5] 5. The semiconductor field-effect device structure of claim 4 wherein the at least one row comprises a plurality of rows.
- [c6] 6. The semiconductor field-effect device structure of claim 1 wherein the engineered array further comprises at least some of the component atoms arranged in a substantially ordered pattern resulting at least in part from self-assembly.
- [c7] 7. The semiconductor field-effect device structure of claim 2 wherein the engineered array further comprises at least some of the component atoms arranged substantially in at least one row.
- [c8] 8. The semiconductor field-effect device structure of claim 7 wherein the at least one row comprises a plurality of rows.

- [c9] 9. The semiconductor field-effect device structure of claim 2 wherein the engineered array further comprises at least some of the component atoms arranged in a substantially ordered pattern resulting at least in part from self-assembly.
- [c10] 10. The semiconductor field-effect device structure of claim 8 wherein the plurality of rows are disposed at least in part to facilitate uniformity of a source-channel interface and a drain-channel interface.
- [c11] 11. The semiconductor field-effect device structure of claim 1 wherein the component atoms comprise p-type dopants.
- [c12] 12. The semiconductor field-effect device structure of claim 1 wherein the component atoms comprise n-type dopants.
- [c13] 13. The semiconductor semiconductor field-effect device structure of claim 1 wherein the component atoms comprise p-type dopants and n-type dopants.
- [c14] 14. The semiconductor field-effect device structure of claim 2 wherein the component atoms comprise p-type dopants.
- [c15] 15. The semiconductor field-effect device structure of

claim 2 wherein the component atoms comprise n-type dopants.

[c16] 16. The semiconductor field-effect device structure of claim 2 wherein the component atoms comprises p-type dopants and n-type dopants.

[c17] 17. A supermolecular structure comprising a host structure and an engineered array of at least one dopant atom disposed at a channel region of the host structure to impart substantial control of a source-drain carrier flow, the supermolecular structure also being described by the formula:

$$H_i Y_1 Y_2 \dots Y_k$$

wherein:

$H$  defines the channel region material;

$i$  is a total number of host matrix atoms;

$Y$  defines the dopant atom type, with  $1$  to  $k$  dopant atom types;

$j$  is the discrete number of dopant atoms of the  $1^{\text{st}}$

dopant atom type in the engineered array; and  
 $l$  is the discrete number of dopant atoms of the  $k^{\text{th}}$   
dopant atom type in the engineered array.

[c18] 18. The supermolecular structure of claim 17 wherein the engineered array further comprises at least some of the at least one atom arranged substantially in at least one row.

[c19] 19. The supermolecular structure of claim 18 wherein the at least one row comprises a plurality of rows.

[c20] 20. The supermolecular structure of claim 18 wherein the engineered array further comprises a substantially ordered pattern of at least some of the at least one dopant atom, the substantially ordered pattern resulting at least in part from self-assembly.

[c21] 21. The supermolecular structure of claim 19 wherein the plurality of rows are disposed at least in part to facilitate uniformity of a source-channel interface and a drain-channel interface.

[c22] 22. A field-effect transistor comprising:  
a source region;  
a drain region;  
a gate structure;  
a first insulator disposed beneath the gate structure and

above the source region and the drain region; and a supermolecular structure disposed beneath the first insulator, the supermolecular structure comprising a host structure and an engineered array of at least one dopant atom disposed at a channel region of the host structure to facilitate substantial control of a source-drain carrier flow, the supermolecular structure also being described by the formula:

$$H_i Y_1 Y_j \dots Y_k Y_l$$

wherein:

$H$  defines the channel region material;

$i$  is a total number of host matrix atoms;

$Y$  defines the dopant atom type, with  $1$  to  $k$  dopant atom types;

$j$  is the discrete number of dopant atoms of the  $1^{\text{st}}$  dopant atom type in the engineered array; and

$l$  is the discrete number of dopant atoms of the  $k^{\text{th}}$  dopant atom type in the engineered array.

prising a second insulator disposed beneath the super-molecular structure so that a silicon-on-insulator (SOI) field-effect transistor is formed.

[c24] 24. The field-effect transistor of claim 22 wherein the engineered array further comprises at least some of the at least one dopant atom arranged substantially in at least one row.

[c25] 25. The field-effect transistor of claim 24 wherein the at least one row comprises a plurality of rows.

[c26] 26. The field-effect transistor of claim 22 wherein the engineered array further comprises at least some of the at least one dopant atom arranged in a substantially ordered pattern resulting at least in part from self-assembly.

[c27] 27. The field-effect transistor of claim 23 wherein the engineered array further comprises at least some of the at least one dopant atom arranged substantially in at least one row.

[c28] 28. The field-effect transistor of claim 27 wherein the at least one row comprises a plurality of rows.

[c29] 29. The field-effect transistor of claim 23 wherein the engineered array further comprises at least some of the

at least one dopant atom arranged in a substantially ordered pattern resulting at least in part from self-assembly.

[c30] 30. The field-effect transistor of claim 25 wherein the plurality rows are disposed at least in part to facilitate uniformity of a source-channel interface and a drain-channel interface.

[c31] 31. The field-effect transistor of claim 28 wherein the plurality of rows are disposed at least in part to facilitate uniformity of a source-channel interface and a drain-channel interface.

[c32] 32. A method of fabricating a field-effect transistor comprising:  
forming a host structure comprising a channel region;  
causing at least one dopant atom to form an engineered array at the channel region;  
growing an epitaxial film over the host structure including the engineered array;  
forming a dielectric layer over the epitaxial film;  
applying a pattern to the host structure including the engineered array of dopant atoms, the epitaxial film, and the dielectric layer to define the final shape of the field-effect transistor; and  
forming a gate electrode atop the dielectric layer.

- [c33] 33. The method of claim 32 wherein the causing of the at least one dopant atom to form the engineered array comprises positioning at least some of the at least one dopant atom using proximity probe manipulation.
- [c34] 34. The method of claim 32 wherein the causing of the at least one dopant atom to form the engineered array comprises positioning at least some of the at least one dopant atom using ion implantation.
- [c35] 35. The method of claim 32 wherein the causing of the at least one dopant atom to form the engineered array comprises facilitating self-assembly of component atoms in a substantially ordered pattern.
- [c36] 36. A method of fabricating a field-effect transistor comprising an engineered array of dopant atoms in a channel region of a host structure, the method comprising:
- forming a semiconductor substrate further comprising the channel region;
  - placing a first atom of the engineered array of dopant atoms on the substrate;
  - growing a first epitaxial film of semiconductor material over the first atom and the semiconductor substrate;
  - continuing to alternately place an additional atom of the

engineered array of dopant atoms and grow an additional epitaxial film of semiconductor on the host structure until the engineered array of dopant atoms is formed beneath a final epitaxial film of semiconductor material;

forming a dielectric layer over the final epitaxial film;

applying a pattern to the host structure including the engineered array of dopant atoms to define the final shape of the field-effect transistor; and

forming a gate electrode atop the dielectric layer.

[c37] 37. The method of claim 36 wherein the placing of at least some of the atoms of the engineered array comprises positioning the at least some of the atoms using proximity probe manipulation.

[c38] 38. The method of claim 36 wherein the placing of at least some of the atoms of the engineered array comprises positioning the at least some of the atoms using ion implantation.